

User's Manual



MSC Q7-TI8168 Module (Texas Instruments® DaVinci™)

Rev. 1.1
January 28th, 2013

Hardware Revision 2.0

Preface

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Content

1 General Information	5
1.1 Revision History	5
1.2 Reference Documents	5
1.3 Signal Terminology	6
1.4 Introduction	6
2 Technical Information	7
2.1 Key features	7
2.2 Jumpers and switches	8
2.3 Watchdog	8
2.4 Power dissipation	8
2.5 Block diagram	9
2.6 LEDs	10
2.7 Signal description	11
2.7.1 PCI Express Lanes	11
2.7.2 Ethernet	12
2.7.3 Serial ATA	13
2.7.4 USB	14
2.7.5 SDIO	15
2.7.6 Audio – I ² S	15
2.7.7 LVDS Flat Panel	16
2.7.8 HDMI	17
2.7.9 LPC Bus	17
2.7.10 SPI Interface	18
2.7.11 Input Power Pins	19
2.7.12 Manufacturing Signals	19
2.7.13 Power and System Management	20
3 System resources	21
3.1 I ² C Bus Address Map	21
4 Mechanical drawing	22
5 Heat spreader	23
6 Boot options	25
6.1 SD Card boot mode and SPI Flash boot mode	25
7 Connectors	26
7.1 Overview	26
7.2 MXM Connector (X1)	27
7.3 Feature Connector (X2)	30
8 Power Domains	32

1 General Information

1.1 Revision History

Rev.	Date	Pages	Description
1.0	1.06.2012	All	Initial Version Hardware Revision 1.0
1.1	28.01.2013	7 8 9 15 18 19 25 31	<ul style="list-style-type: none">- Audio compatibility updated- Power dissipation details added- SPI Flash added to block diagram- Added SDIO signals pull-ups, audio signals updated to I²S- SPI_CS1# signal not supported on Feature connector- Added note for JTAG signals- Boot options updated- SPI_CS1# signal removed from Feature connector

1.2 Reference Documents

[1] Qseven Specification
Revision 2.0
Last update: September 20th 2012
<http://www.Qseven-standard.org>

1.3 Signal Terminology

- Signal direction: Signal directions are from the module perspective.
For example: COM_TXD (serial port transmit) is an output from the CPU module
- The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is active at a high voltage level
- Differential pairs are indicated by trailing “+” and “-“ signs for the positive or negative signal

1.4 Introduction

The MSC Q7-TI8168 is part of the MSC Qseven[®] family of Qseven[®] CPU modules. It is based on a Texas Instruments[®] DaVinci[™] System-on-a-Chip (SoC) which incorporates a high performance ARM[®] Cortex[™] A8 RISC MPU together with TI's C674x VLIW DSP core.

The module is fully compliant with the Qseven[®] Specification Revision 2.0.

All functionalities are listed in the Technical Information section. Depending on the assembly variant different subsets are available.

2 Technical Information

2.1 Key features

CPU	ARM® Cortex™ A8 processor, 1,2GHz <ul style="list-style-type: none"> ■ 32KB instruction and data caches ■ 256KB L2 cache ■ 64KB RAM, 48KB boot ROM C674x floating/fixed point DSP operating up to 1 GHz <ul style="list-style-type: none"> ■ Up to 8000/6000 C674x MIPS/MFLOPS
Memory	32-bit DDR3, 800MHz, 1GByte
Audio-Video Processor HD	Three HDVICP2 hardware accelerator subsystems supports resolutions up to 1080 p/i with full performance of 60 fps <ul style="list-style-type: none"> ■ MPEG4 encoding & decoding ■ MPEG2 encoding & decoding ■ MPEG1 encoding & decoding ■ H.264 encoding & decoding ■ DivX 5.x and higher, encoding & decoding ■ RV/ON2 decoding ■ AVS 1.0 encoding & decoding ■ WMV9/ VC1/RTV encoding & decoding ■ JPEG/MJPEG encoding & decoding
Dual Display Controller	<ul style="list-style-type: none"> ■ HDMI 1.3 – Full HD (1080p) ■ LCD (single channel 24bpp) – up to WXGA+ (1440 x 900 @ 60Hz)
Video input	8 bit YCbCr video input up to 165MHz (available on feature connector)
GPU	SGX530 3D Graphics Engine <ul style="list-style-type: none"> ■ Delivers up to 30 MTriangles/s ■ Direct3D® Mobile, OpenGL® ES 1.1 and 2.0, ■ OpenVG™ 1.1, OpenMax™ API Support
Ethernet	Lantiq® XWAY PEF7072, IEEE 802.3 compliant (10/100/1000)
PCI Express	One x1 PCIe 1.1 port
Audio	I ² S compatible
USB	Integrated 2 ports USB 2.0 Controller (1x Host, 1x Host/Client), PCIe to USB Swidge for 4 additional USB 2.0 ports
SATA	2 SATA 3.0 interfaces

Serial, SPI, I²C	<ul style="list-style-type: none"> ■ 2 integrated UART Controllers (1 on feature connector) ■ integrated SPI Controller (3 slave selects, 1 on feature connector) ■ integrated I²C Controller
Flash Memory	<ul style="list-style-type: none"> ■ NAND Flash, 2GB (8Bit data bus) ■ SPI Flash, 4 MB, 40 MHz
SDIO	Integrated 4 bit SD/MMC Controller (SD, MMC, SDHC, SDIO), maximum frequency 48MHz
RTC	RTC with I ² C-Interface (typ. Power Consumption 350nA @ 3V)
Boot sources*	<ul style="list-style-type: none"> ■ NAND Flash ■ SPI Flash ■ SD Card ■ Ethernet
Power Supply	5V (4,75V – 5,25V) 5V (4,75V – 5,25V) Standby voltage 3V (1,3V – 3,3V) <i>optionally for RTC</i>

*U-boot must be resident on the SPI Flash or the SD Card

2.2 Jumpers and switches

There are no jumpers or switches on the module.

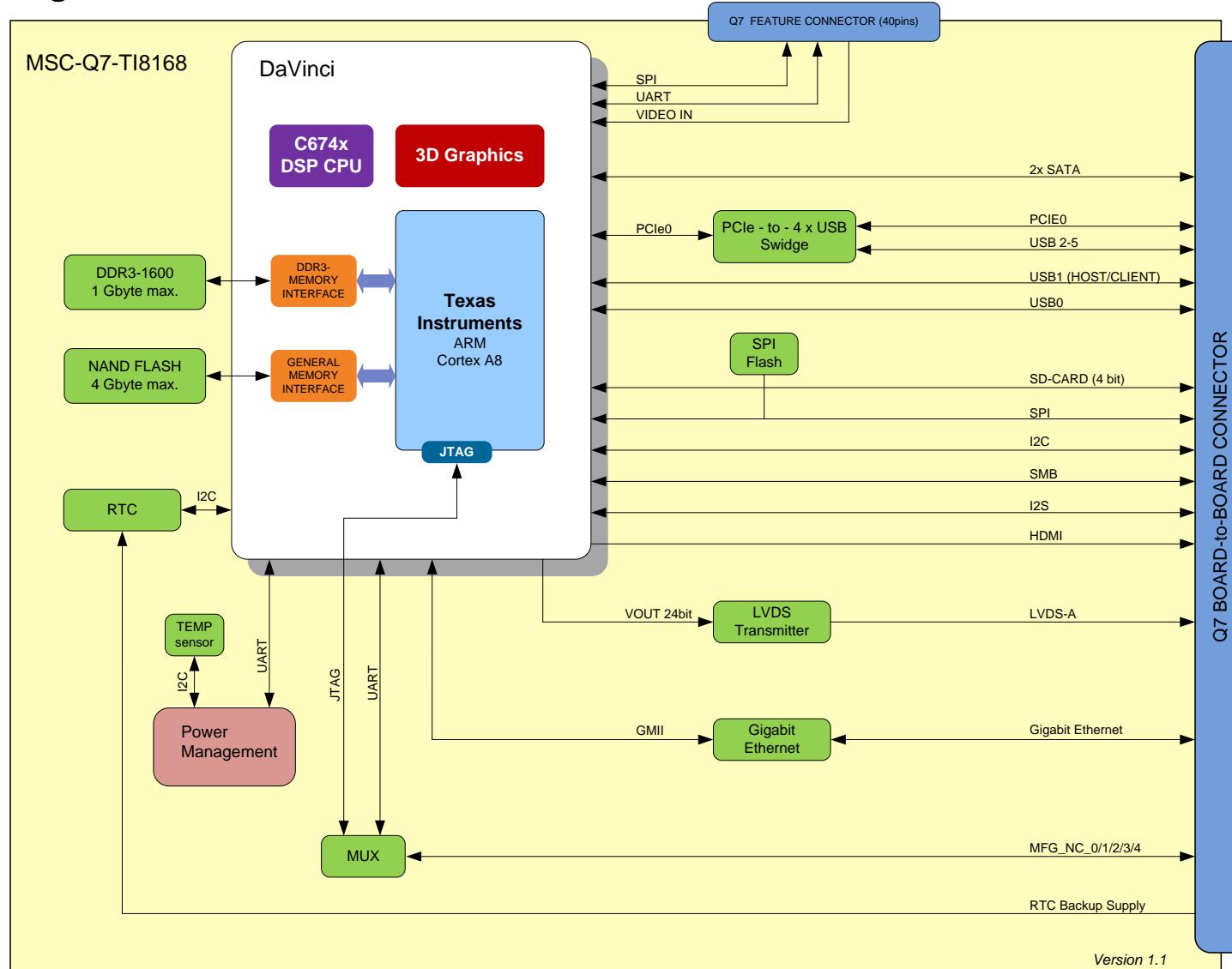
2.3 Watchdog

t.b.d

2.4 Power dissipation

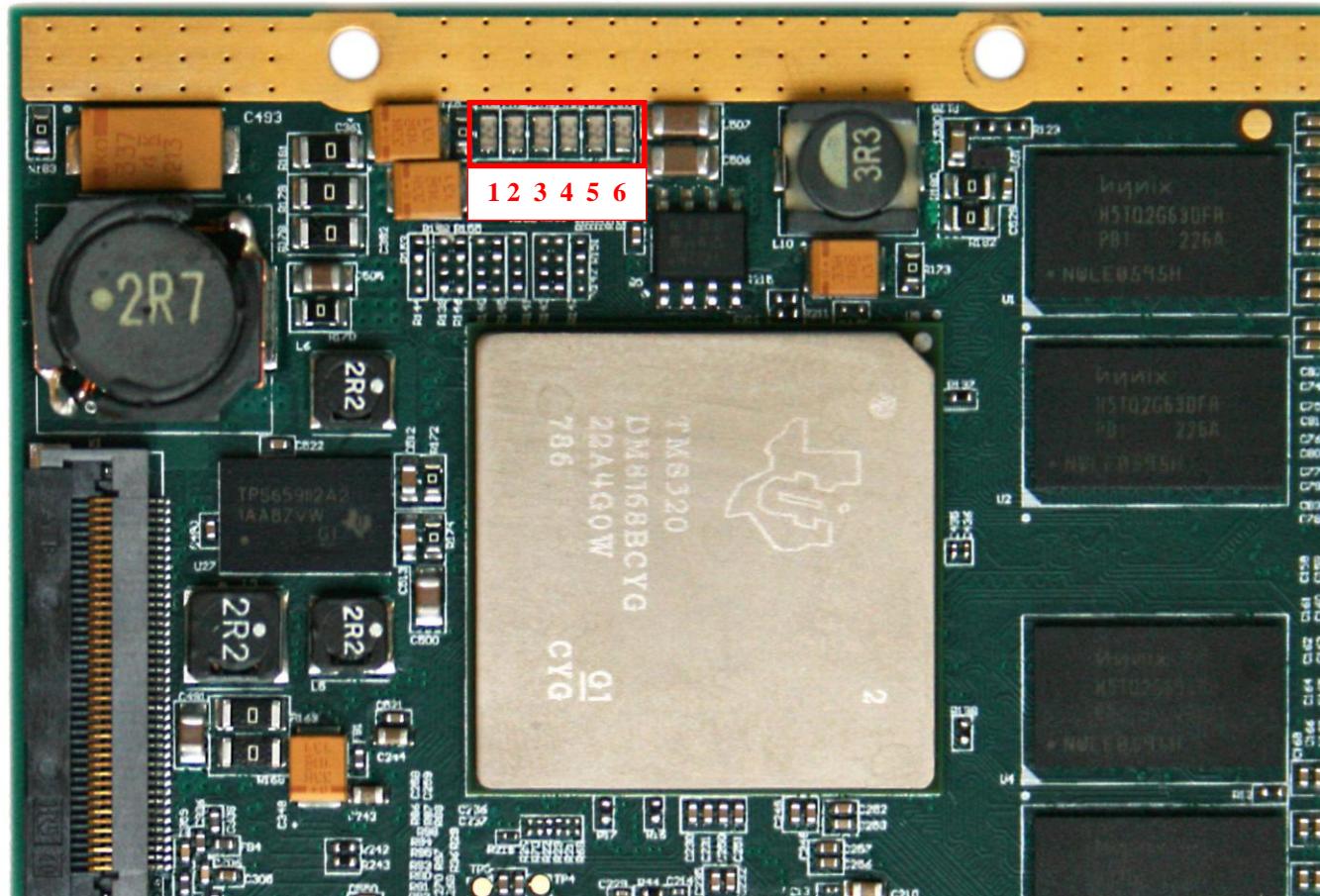
Mode	Voltage	Current	Power	Description
Idle	5V	1.655 A	8.275 W	Measured at the login prompt ten minutes after booting
CPU tests	5V	1.823 A	9.115 W	Measured while running CPU tests fifteen minutes after booting (LINPACK CPU test)
HD video	5V	1.9 A	9.5 W	Measured while decoding HD video (hardware accelerated) two minutes after rebooting

2.5 Block diagram



2.6 LEDs

There are six onboard LEDs. All of them are available as USER LEDs.



2.7 Signal description

In the following tables signals are marked with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different.

An additional label, “Suspend”, indicates that the pin is active during suspend states (S3, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.7.1 PCI Express Lanes

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCIE0_TX+	O	PCIe	CPU	AC coupled on module		PCI Express 1.1 Differential Transmit Pairs 0	DaVinci
PCIE0_RX+	I	PCIe	CPU	Requires AC coupling on baseboard		PCI Express 1.1 Differential Receive Pairs 0	/ DaVinci
PCIE_CLK_REF+	O	PCIe	CPU	AC coupled on module		PCI Express Reference Clock for Lane 0	Clock generator
PCIE_RST#	O	CMOS	CPU	3.3V	5k1 PD	Reset Signal for external devices.	PCIe-to-USB Swidge

2.7.2 Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description				Source / Target																																					
GBE_MDI[0:3]+	Input/ Output	Analog	Suspend			Gigabit Ethernet Controller: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes.				Gigabit Ethernet Controller																																					
GBE_MDI[0:3]-						<p>1000BASE-T</p> <table border="1"> <thead> <tr> <th colspan="2">MDI configuration:</th><th colspan="2">MDI-X configuration:</th></tr> </thead> <tbody> <tr><td>MDI[0]+/-</td><td>BI_DA+/-</td><td>MDI[0]+/-</td><td>BI_DB+/-</td></tr> <tr><td>MDI[1]+/-</td><td>BI_DB+/-</td><td>MDI[1]+/-</td><td>BI_DA+/-</td></tr> <tr><td>MDI[2]+/-</td><td>BI_DC+/-</td><td>MDI[2]+/-</td><td>BI_DC+/-</td></tr> <tr><td>MDI[3]+/-</td><td>BI_DD+/-</td><td>MDI[3]+/-</td><td>BI_DD+/-</td></tr> </tbody> </table> <p>100BASE-TX/ 10BASE-T</p> <table border="1"> <thead> <tr> <th colspan="2">MDI configuration:</th><th colspan="2">MDI-X configuration:</th></tr> </thead> <tbody> <tr><td>MDI[0]+/-</td><td>Transmit</td><td>MDI[0]+/-</td><td>Receive</td></tr> <tr><td>MDI[1]+/-</td><td>Receive</td><td>MDI[1]+/-</td><td>Transmit</td></tr> <tr><td>MDI[2]+/-</td><td>unused</td><td>MDI[2]+/-</td><td>unused</td></tr> <tr><td>MDI[3]+/-</td><td>unused</td><td>MDI[3]+/-</td><td>unused</td></tr> </tbody> </table>					MDI configuration:		MDI-X configuration:		MDI[0]+/-	BI_DA+/-	MDI[0]+/-	BI_DB+/-	MDI[1]+/-	BI_DB+/-	MDI[1]+/-	BI_DA+/-	MDI[2]+/-	BI_DC+/-	MDI[2]+/-	BI_DC+/-	MDI[3]+/-	BI_DD+/-	MDI[3]+/-	BI_DD+/-	MDI configuration:		MDI-X configuration:		MDI[0]+/-	Transmit	MDI[0]+/-	Receive	MDI[1]+/-	Receive	MDI[1]+/-	Transmit	MDI[2]+/-	unused	MDI[2]+/-	unused	MDI[3]+/-
MDI configuration:		MDI-X configuration:																																													
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MDI configuration:		MDI-X configuration:																																													
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MDI[2]+/-	unused	MDI[2]+/-	unused																																												
MDI[3]+/-	unused	MDI[3]+/-	unused																																												
GBE_ACT#	OD	CMOS	CPU	3.3V		Gigabit Ethernet Controller: activity indicator, active low.				Logic																																					
GBE_LINK#	OD	CMOS	CPU	3.3V		Gigabit Ethernet Controller: link indicator, active low.				Logic																																					
GBE_LINK100#	OD	CMOS	CPU	3.3V		Gigabit Ethernet Controller: 100 Mbit / sec link indicator, active low.				Logic																																					
GBE_LINK1000#	OD	CMOS	CPU	3.3V		Gigabit Ethernet Controller: 1000 Mbit / sec link indicator, active low.				Logic																																					
GBE_CTREF	REF			GND min 3.3V max		Gigabit Ethernet Controller (1000MBit) : unconnected				Unconnected / Not required																																					

2.7.3 Serial ATA

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA0_TX+	O	SATA	CPU	AC coupled on module		Serial ATA Channel 0: differential transmit pair.	DaVinci
SATA0_RX+	I	SATA	CPU	AC coupled on module		Serial ATA Channel 0: differential receive pair.	/ DaVinci
SATA1_TX+	O	SATA	CPU	AC coupled on module		Serial ATA Channel 1: differential transmit pair.	DaVinci
SATA1_RX+	I	SATA	CPU	AC coupled on module		Serial ATA Channel 1: differential receive pair.	/ DaVinci
SATA_ACT#	OD	CMOS	CPU	3.3V		SATA activity indicator (both channels), active low. External Pullup has to be installed on Carrier Board.	Logic

2.7.4 USB

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
USB_P0+ USB_P0-	I/O	USB	CPU			USB differential pair, channels 0	DaVinci
USB_P1+ USB_P1-	I/O	USB	CPU			USB differential pair, channels 1 This port may be optionally used as USB client port.	DaVinci
USB[2:5]+ USB[2:5]-	I/O	USB	CPU			USB differential pairs, channels 2 to 5	PCIe-to-USB Swidge
USB_0_1_OC#	I	CMOS	CPU	3.3V	1k43 PU	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	DaVinci
USB_2_3_OC#	I	CMOS	CPU	3.3V	4k7 PU	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	/ PCIe-to-USB Swidge
USB_4_5_OC#	I	CMOS	CPU	3.3V	4k7 PU	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	/ PCIe-to-USB Swidge
USB_ID	I	CMOS	CPU	3.3V		USB ID pin. High signal level configures USB Port1 (and CPU) as USB Client	/ DaVinci
USB_CC	I	CMOS	CPU	3.3V		USB client connect pin.	/ DaVinci

2.7.5 SDIO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDIO_DAT[0:3]	I/O	3.3V	CPU	3.3V	10k PU	SDIO Controller Data	DaVinci
SDIO_CD#	I	3.3V	CPU	3.3V		SDIO Controller Card Detect	/ DaVinci
SDIO_CMD	I/O	3.3V	CPU	3.3V	10k PU	SDIO Controller Command	DaVinci
SDIO_CLK	O	3.3V	CPU	3.3V	10k PU	SDIO Controller Clock	DaVinci
SDIO_PWR#	I/O	3.3V	CPU	3.3V	10k PU	SDIO Controller Power enable	Logic
SDIO_LED	O	3.3V	CPU	3.3V	10k PD	SDIO Controller transfer activity LED	DaVinci
SDIO_WP	I	3.3V	CPU	3.3V		SDIO Controller Write Protect	/ DaVinci

2.7.6 Audio – I²S

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
I2S_RST#	Output	CMOS	CPU	3.3V	10k PD	Reset output to CODEC, active low	DaVinci
I2S_WS	Output	CMOS	CPU	3.3V		I2S Word Select output	DaVinci
I2S_CLK	Output	CMOS	CPU	3.3V		I2S Serial Data Clock to CODEC	DaVinci
I2S_SDO	Output	CMOS	CPU	3.3V		Serial Data Output to CODEC	DaVinci
I2S_SDI	Input	CMOS	CPU	3.3V		Serial Data Input from CODEC	/ DaVinci

2.7.7 LVDS Flat Panel

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_A[0:3]+	O	LVDS	CPU			LVDS Channel A differential pairs – primary channel	LVDS Transmitter
LVDS_A[0:3]-							
LVDS_A_CLK+	O	LVDS	CPU			LVDS Channel A differential clock	LVDS Transmitter
LVDS_A_CLK-							
LVDS_PPEN	O	CMOS	CPU	3.3V		LVDS panel power enable	DaVinci
LVDS_BLEN	O	CMOS	CPU	3.3V	10k PD	LVDS panel backlight enable	DaVinci
LVDS_BLT_CTRL	O	CMOS	CPU	3.3V		LVDS panel backlight brightness control	DaVinci
LVDS_DID_CLK	I/O OD	CMOS	CPU	3.3V	1k43 PU	I2C clock output for LVDS display use	I2C Switch
LVDS_DID_DAT	I/O OD	CMOS	CPU	3.3V	1k43 PU	I2C data line for LVDS display use	I2C Switch

2.7.8 HDMI

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
TMDS_LANE0+	O	HDMI	CPU			TMDS differential pair lines lane 0	DaVinci
TMDS_LANE0-	O	HDMI	CPU			TMDS differential pair lines lane 1	DaVinci
TMDS_LANE2+	O	HDMI	CPU			TMDS differential pair lines lane 2	DaVinci
TMDS_CLK+	O	HDMI	CPU			TMDS differential pair clock lines	DaVinci
HDMI_HPD#	I	CMOS	CPU		10k PD	Hot plug detection signal that serves as an interrupt request. Signal can only be pulled to a logic low level.	/ DaVinci
HDMI_CTRL_CLK	I/O OD	CMOS	CPU	3.3V	40k2 PU	DDC based control signal (clock) for HDMI device	DaVinci
HDMI_CTRL_DAT	I/O OD	CMOS	CPU	3.3V	40k2 PU	DDC based control signal (data) for HDMI device	DaVinci

2.7.9 LPC Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LPC_FRAME#	O	CMOS	CPU	Not supported		Not supported	Not supported
LPC_CLK	O	CMOS	CPU	Not supported		Not supported	Not supported

2.7.10 SPI Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SPI_MOSI	O	CMOS	CPU	3.3V		Master serial output / Slave input signal – CPU is master	Logic
SPI_MISO	I	CMOS	CPU	3.3V		Master serial input / Slave output signal – CPU is master	/ Logic
SPI_SCK	O	CMOS	CPU	3.3V		SPI clock input	Logic
SPI_CS0#	O	CMOS	CPU	3.3V	5k1 PU	SPI chip select 1 output, active low (chip select for primary device) on Qseven connector	DaVinci
SPI_CS1#	O	CMOS	CPU	3.3V	5k1 PU	SPI chip select 2 output, active low (chip select for secondary device) on Qseven connector	DaVinci
SPI_CS2#	O	CMOS	CPU	3.3V	5k1 PU	SPI chip select 3 output, active low (chip select for primary device) on Feature connector	DaVinci

2.7.11 Input Power Pins

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VCC	Power		5V	(±5%)		Primary power input: +5V (±5%)	/ Voltage Regulators
VCC_5V_SB	Power		5V	(±5%)		Standby power input: +5.0V (±5%) All available VCC5V0_STBY pins on the connector(s) shall be used. Used for microcontroller and standby and suspend functions. NOTE: If the baseboard does not provide the VCC_5V_SB then these pins should be connected to the main VCC power supply on the baseboard!	/ Voltage Regulators
VCC_RTC	Power					Real-time clock circuit-power input : +3.0V (+1.3V to +3.3V)	/ RTC
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.7.12 Manufacturing Signals

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
MFG_NC0 ¹	I	CMOS	CPU	3.3V		Boundary Scan – TCK	/ DaVinci
MFG_NC1	O	CMOS	CPU	3.3V		Boundary Scan – TDO / COM_TXD: Depending on MFG_NC4 the signal is either used as Boundary Scan TDO or as transmit signal for the serial debug port (UART)	DaVinci
MFG_NC2	I	CMOS	CPU	3.3V		Boundary Scan – TDI / COM_RXD: Depending on MFG_NC4 the signal is either used as Boundary Scan TDI or as receive signal for the serial debug port (UART)	/ DaVinci
MFG_NC3	I	CMOS	CPU	3.3V		Boundary Scan – TMS	/ DaVinci
MFG_NC4 ²	I	CMOS	CPU	3.3V	4k7 PD	Control Signal for multiplexer circuit: 1: Boundary Scan / JTAG 0: UART	/ DaVinci

¹ On some JTAG debuggers, which require return clock from processor, pins TCK and RCK should be connected (pins 11 and 9 on Standard TI 14-pin JTAG Header).

² This signal should have defined default logic level (pull-up or pull-down resistor on the carrier board).

2.7.13 Power and System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PWRBTN#	I	CMOS	Suspend	3.3V	10k PU	Power button to bring system into a power state, active low (negative pulse, 6 seconds power override)	/Microcontroller
RSTBTN#	I	CMOS	Suspend	3.3V	10k PU	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release. (negative pulse)	/Microcontroller
SUS_STAT#	O	CMOS				Not supported.	Not supported.
SUS_S3#	O	CMOS	Suspend	3.3V	10k PD	Indicates that the system is in Soft Off state. Can be used to control an ATX power supply.	Microcontroller
SUS_S5#	O	CMOS	Suspend	3.3V	10k PD	Indicates that the system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	Microcontroller
LID_BTN#	I	CMOS				Not supported.	Not supported.
SLP_BTN#	I	CMOS				Not supported.	Not supported.
BATLOW#	I	CMOS	Suspend	3.3V	10k PU	Signal that indicates that the system battery is low.	/Microcontroller
WAKE#	I	CMOS				Not supported.	Not supported.
THRM#	I	CMOS	Suspend	3.3V		Input from off-module temp sensor indicating an over-temp situation.	/Microcontroller
THERMTRIP#	O	CMOS	Suspend	3.3V		Active low output indicating that the CPU has entered thermal shutdown.	Microcontroller
PWGIN	I	5V CMOS	Suspend	5V		Indicates that the external power supply is ready	/Microcontroller
WDOUT	O	CMOS	CPU	3.3V		Output indicating that a watchdog time-out event has occurred.	DaVinci
WDTRIG#	I	CMOS	CPU	3.3V	10k PU	Watchdog trigger input. This signal restarts the watchdog timer	DaVinci
GP_TIMER_IN	I	CMOS	Suspend	3.3V		General purpose timer input	/Microcontroller
GP_PWM_OUT1	OD	CMOS	Suspend	3.3V		General purpose PWM output	Microcontroller
SPKR	O	CMOS	CPU	3.3V	10k PD	Output for audio enunciator.	DaVinci
SMB_CLK*	I/O	CMOS	CPU	3.3V	10k PU	System management clock line	Microcontroller
SMB_DAT	I/O	CMOS	CPU	3.3V	10k PU	System management data line	Microcontroller
SMB_Alert	I/O	CMOS	CPU	3.3V	10k PU	System management bus alert input	Microcontroller
I2C_CLK	I/O	CMOS	CPU	3.3V	1k43 PU	General purpose I2C port clock output	I2C Switch
I2C_DAT	I/O	CMOS	CPU	3.3V	1k43 PU	General purpose I2C port data I/O line	I2C Switch

*SMBus covers complete address range

3 System resources

3.1 I2C Bus Address Map

The on-board I2C switch splits the I2C bus into two branches:

- Qseven on-module I2C
- System I2C going to the Qseven connector

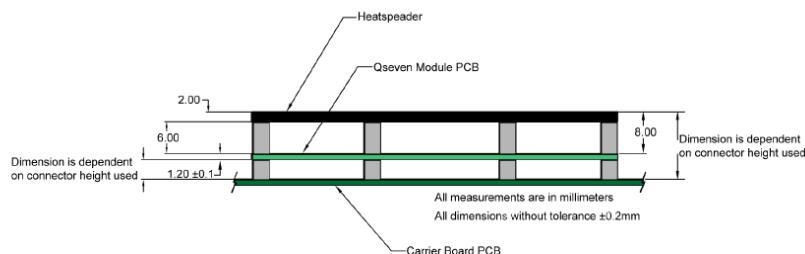
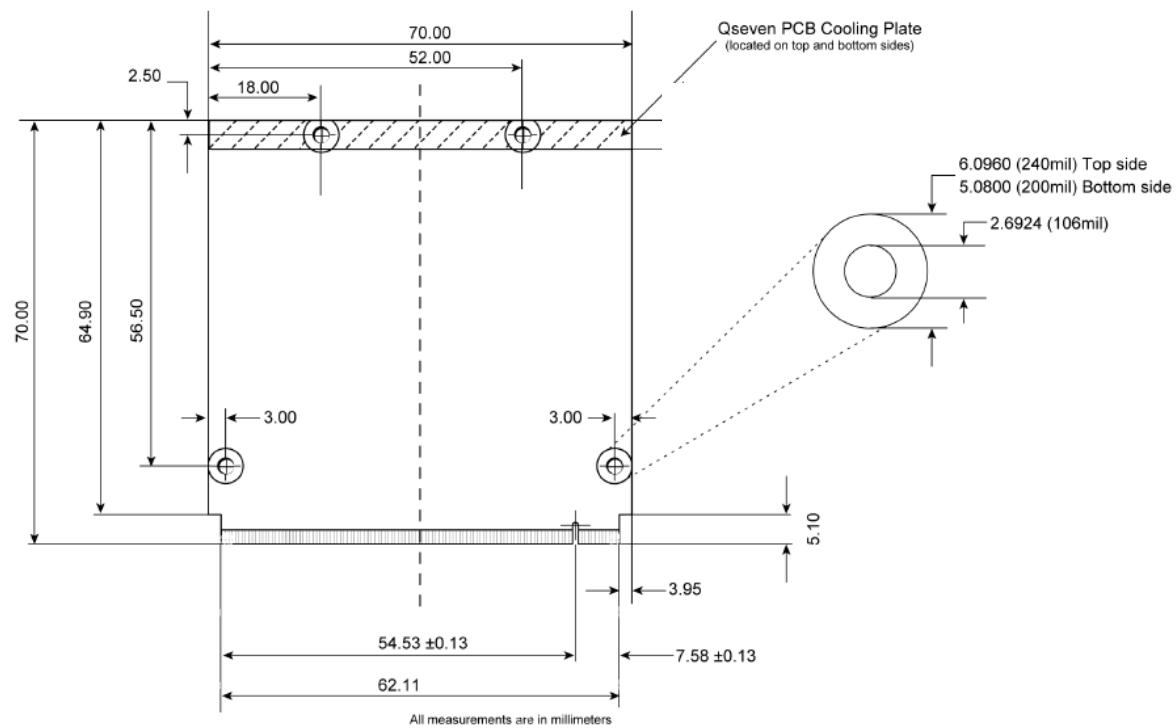
Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
I2C Switch	1	1	1	0	0	0	0	x	E0 _h / E1 _h

Available devices on Qseven on-module branch:

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
ID-EEPROM	1	0	1	0	0	0	0	x	A0 _h / A1 _h
RTC	1	1	0	1	0	0	0	x	D0 _h / D1 _h

*) 8 bit address R/W

4 Mechanical drawing



The actual height depends on the Qseven connector used on the baseboard.

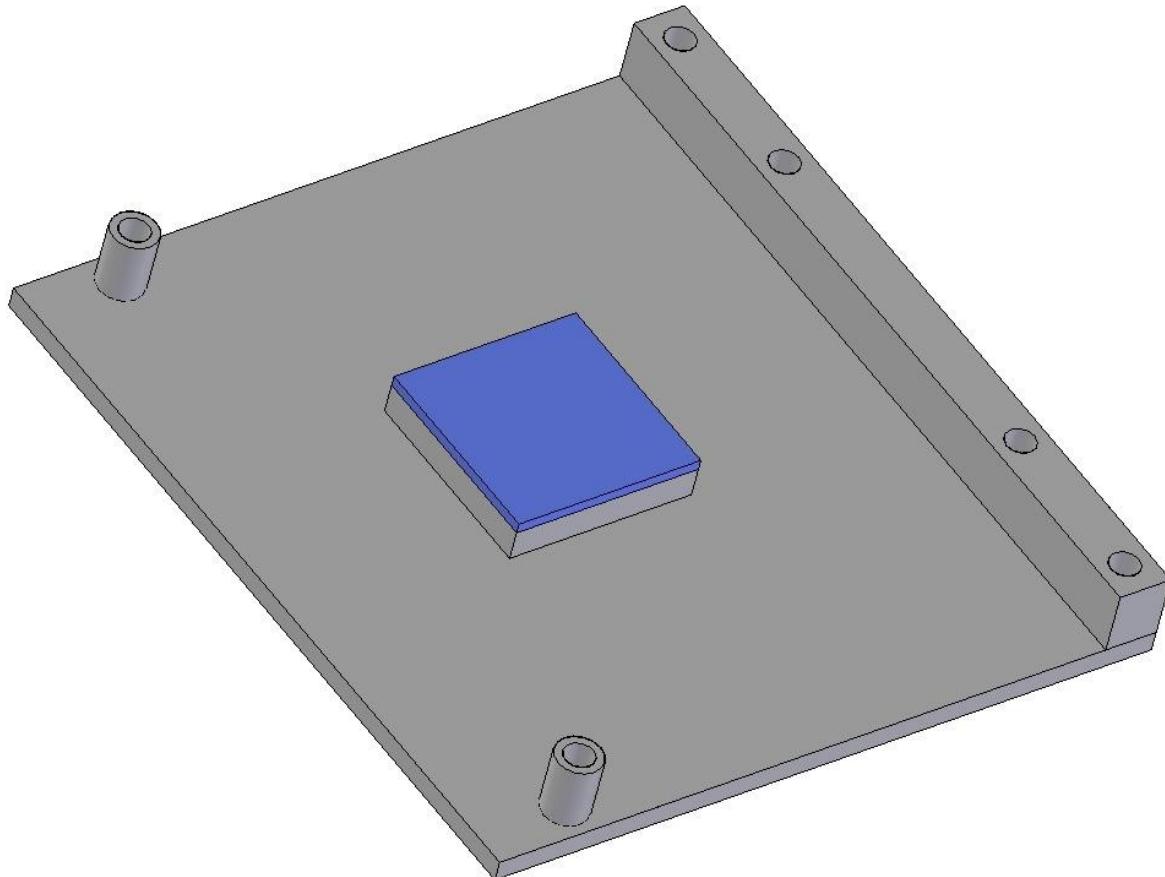
5 Heat spreader

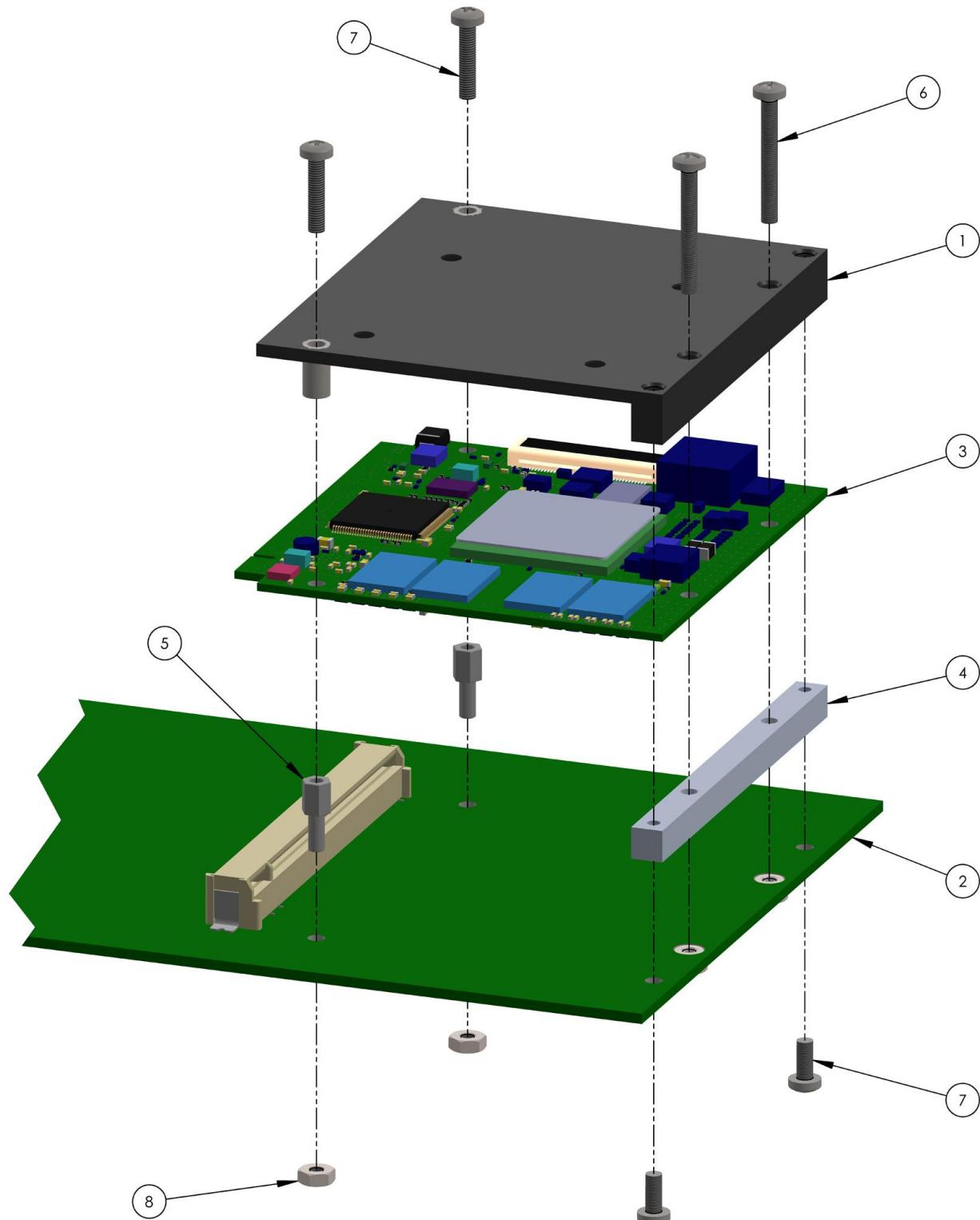
The cooling solution for a Qseven module is based on a heat spreader concept. The purpose of the heat spreader is to provide a standard thermal interface.

A heat spreader is a metal plate (typically aluminium) mounted on top of the module. Its mechanical dimensions follow the module standard specification. The connection between the metal plate and the thermal active components on the module is typically made via thermal interface materials such as phase change foils, gap pads and metal blocks. A good thermal conductivity is required in order to transfer the heat from the hotspots to the heat spreader plate.

The heat spreader used for the MSC Q7-TI8168 CPU module is thermally attached using phase change materials and a small aluminium block that is part of the heat spreader plate.

Usage of the heat spreader is obligatory, but there might be applications that require additional type of cooling solution together with heat spreader (passive casing heat dissipation or cooling fan). In any case it is the system designer's responsibility to make sure that each device in the system operates within its specified thermal limits. The cooling solution should ensure that the thermal specifications for each component are met over the full operating range of the system.





Bill of Material		
Pos-Nr.	Description	Qty
1	MSC Q7-TI8168-01 HSP-001	1
2	Q7 Mainboard	1
3	MSC Q7-TI8168	1
4	MEC Q7 COOLSTRIP ALU 70x5x5	1
5	MEC BOLT HEX-M/F M2.5 SW4 L5	2
6	MEC Screw Fillister Head M2.5x20 Cross	2
7	MEC Screw Fillister Head M2.5x6 Cross	2
8	MEC NUT HEX M2.5 SW5 m2.0	2

6 Boot options

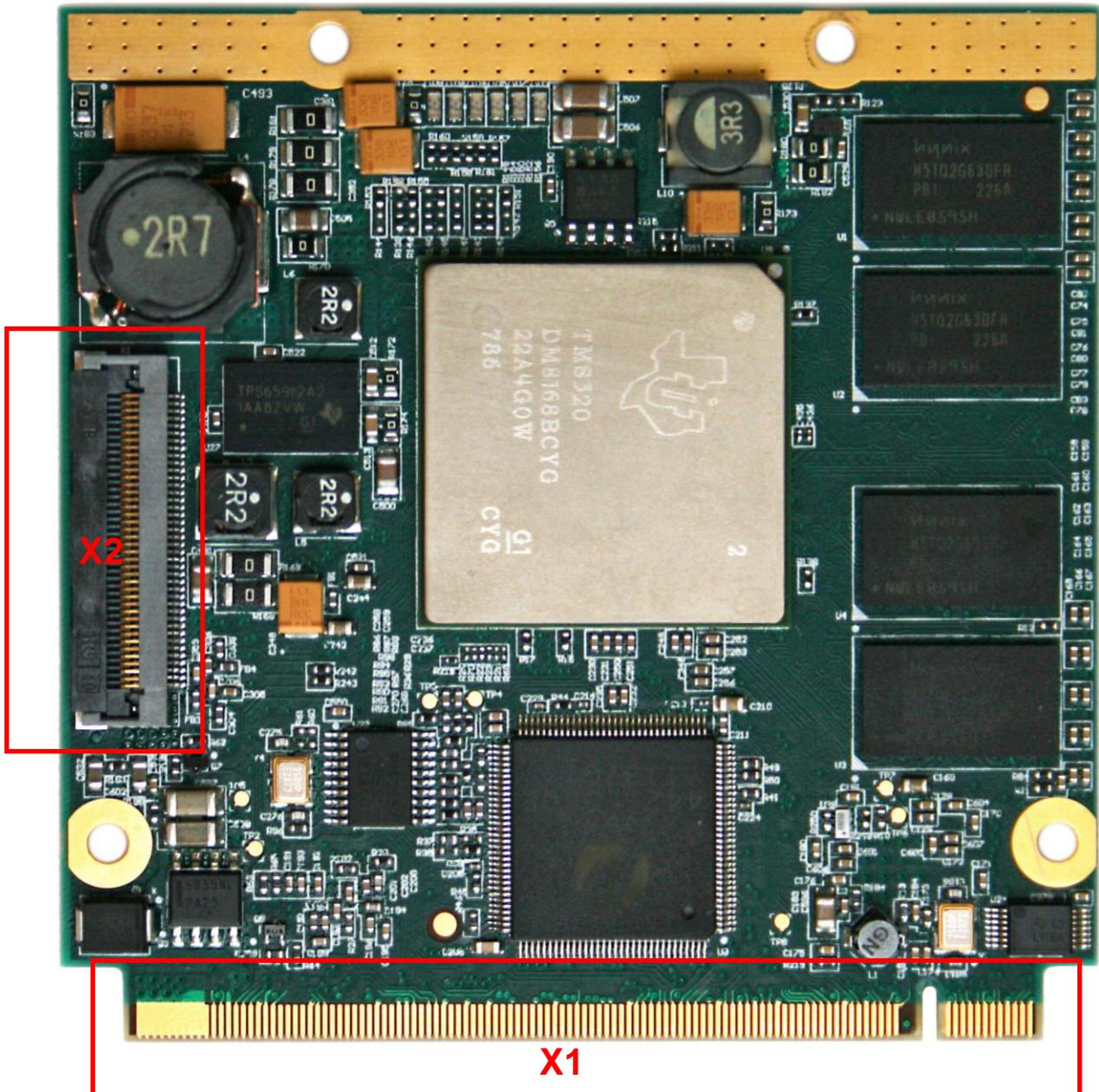
The MSC Q7-TI8168 has several booting options.

6.1 SD Card boot mode and SPI Flash boot mode

SD card boot is of higher priority than SPI Flash boot. If a card is present but doesn't contain a valid bootloader, the CPU will skip to SPI Flash. Subsequently the kernel can be loaded from Ethernet, NAND Flash or SD Card.

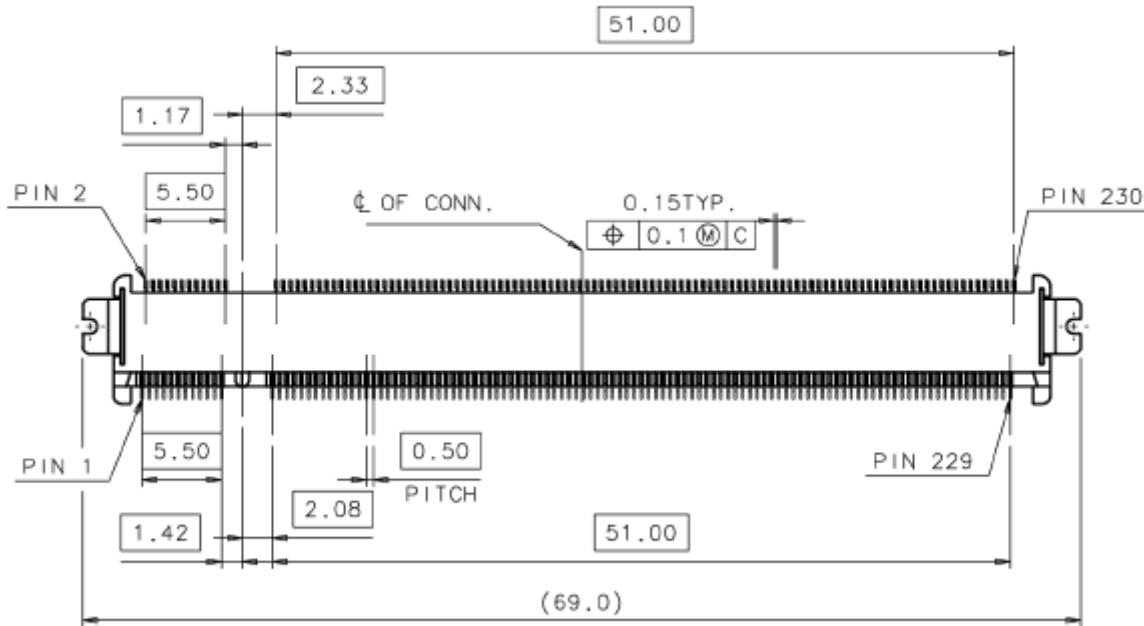
7 Connectors

7.1 Overview



	Function	Description
X1	Qseven Finger – 230pins	Qseven edge contacts to connect to MXM connector (refer to Qseven specification)
X2	Qseven Feature Connector – 40pins	Optional Qseven I/O-Connector with additional features

7.2 MXM Connector (X1)



NOTE: Signals in grey are not available on the MSC-Q7-TI8168 module

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
KEY			
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5

53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	RSVD
57	GND	58	GND
59	HDA_SYNC / I2S_WS	60	SMB_CLK
61	HDA_RST# / I2S_RST#	62	SMB_DAT
63	HDA_BITCLK / I2S_CLK	64	SMB_ALERT#
65	HDA_SDI / I2S_SDI	66	I2C_CLK
67	HDA_SDO / I2S_SDO	68	I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTrip#	72	WDOUT
73	GND	74	GND
75	USB_P7-	76	USB_P6-
77	USB_P7+	78	USB_P6+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5-	82	USB_P4-
83	USB_P5+	84	USB_P4+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CC	92	USB_ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	LVDS_A0+	100	LVDS_B0+
101	LVDS_A0-	102	LVDS_B0-
103	LVDS_A1+	104	LVDS_B1+
105	LVDS_A1-	106	LVDS_B1-
107	LVDS_A2+	108	LVDS_B2+
109	LVDS_A2-	110	LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	LVDS_A3+	114	LVDS_B3+
115	LVDS_A3-	116	LVDS_B3-
117	GND	118	GND
119	LVDS_A_CLK+	120	LVDS_B_CLK+
121	LVDS_A_CLK-	122	LVDS_B_CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	124	RSVD
125	LVDS_DID_DAT / GP_I2C_DAT	126	LVDS_BLC_DAT
127	LVDS_DID_CLK / GP_I2C_CLK	128	LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	SDVO_BCLK+ / HDMI_TMDS_CLK+	132	SDVO_INT+
133	SDVO_BCLK- / HDMI_TMDS_CLK-	134	SDVO_INT-
135	GND	136	GND
137	SDVO_GREEN+ / HDMI_TMDS_LINE1+	138	SDVO_FLDSTALL+
139	SDVO_GREEN- / HDMI_TMDS_LINE1-	140	SDVO_FLDSTALL-
141	GND	142	GND
143	SDVO_BLUE+ / HDMI_TMDS_LINE0+	144	SDVO_TVCLKIN+
145	SDVO_BLUE- / HDMI_TMDS_LINE0-	146	SDVO_TVCLKIN-
147	GND	148	GND
149	SDVO_RED+ / HDMI_TMDS_LINE2+	150	SDVO_CTRL_DAT / HDMI_CTRL_DAT
151	SDVO_RED- / HDMI_TMDS_LINE2-	152	SDVO_CTRL_CLK / HDMI_CTRL_CLK

153	HDMI_HPD#	154	DP_HPD#
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_RX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_RX-	170	PCIE2_RX-
171	EXCD0_PERST#	172	EXCD1_PERST#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_RX-	176	PCIE1_RX-
177	EXCD0_CPPE#	178	EXCD1_CPPE#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_RX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

7.3 Feature Connector (X2)

X2 is an optional connector with extra features. It's located on the top side of the module and it's power domain is CPU.

The following features are supported:

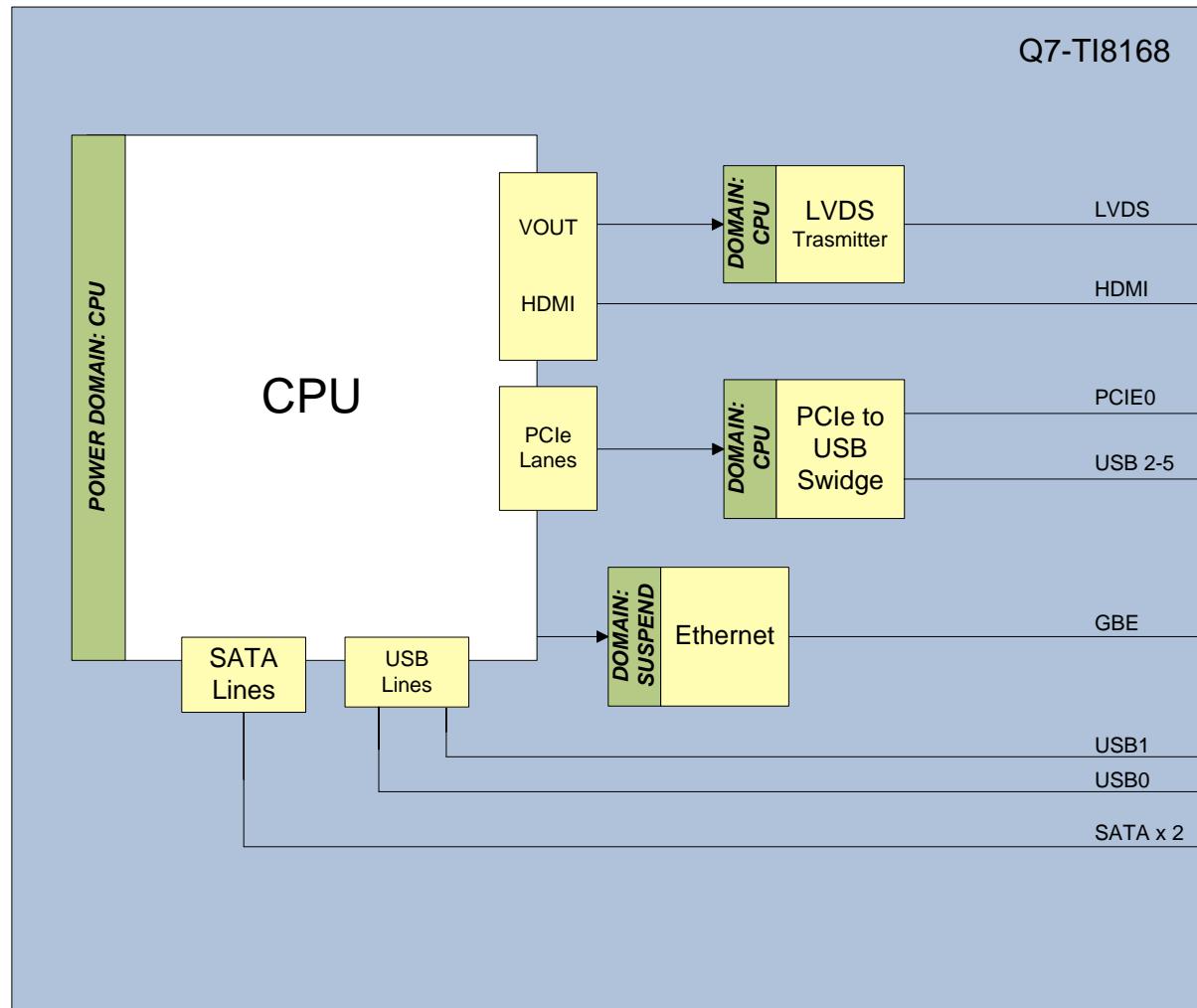
- Serial Port (LVTTL):
A serial port with hardware handshaking (RTS, CTS) is also provided. An external transceiver is necessary for RS232, for example.
- Video capture port:
8 bit YCbCr video input up to 165MHz.
- SPI interface (same SPI data lines as on Qseven conn. with one separate chip select):
4 wire interface with one low active chip select. The Qseven module is master.

Type: 40 pin FPC connector, 0.5mm pitch, Hirose FH28-40S-0.5SH

Pin	Signal	Description	I/O
1	CAM_D0	Camera Data Bit 0	IN
2	CAM_D1	Camera Data Bit 1	IN
3	CAM_D2	Camera Data Bit 2 (<i>LSB in 8 Bit mode – YCbCr</i>)	IN
4	CAM_D3	Camera Data Bit 3	IN
5	CAM_D4	Camera Data Bit 4	IN
6	CAM_D5	Camera Data Bit 5	IN
7	CAM_D6	Camera Data Bit 6	IN
8	CAM_D7	Camera Data Bit 7	IN
9	CAM_D8	Camera Data Bit 8	IN
10	CAM_D9	Camera Data Bit 9 (<i>MSB in 8 Bit (YCbCr) mode</i>)	IN
11	GND	Signal ground	-
12	CAM_SHFCLK	Camera pixel clock	IN
13	CAM_MCLK	Camera master reference clock	OUT
14	CAM_VSYNC	Camera vertical sync	IN
15	CAM_HSYNC	Camera horizontal sync	IN
16	CAM_GPIO0	Camera GPIO (<i>imager reset</i>)	IN/ OUT
17	CAM_GPIO1	Camera GPIO (<i>optional PWM output</i>)	IN/ OUT
18	CAM_I2C_SDA	Camera I2C Data	IN/ OUT
19	CAM_I2C_SCL	Camera I2C Clock	OUT
20	GND	Signal Ground	-
21	COM_TXD	Serial Port – Transmit Data (<i>LVTTL</i>)	OUT
22	COM_RXD	Serial Port – Receive Data (<i>LVTTL</i>)	IN
23	COM_RTS#	Serial Port – Ready to send (<i>LVTTL – low active</i>)	OUT
24	COM_CTS#	Serial Port – Clear to send (<i>LVTTL – low active</i>)	IN
25	GND	Signal Ground	-
26	VGA_R	VGA output – RED component	OUT
27	VGA_G	VGA output – GREEN component	OUT

28	VGA_B	VGA output – BLUE component	OUT
29	VGA_HSYNC	VGA horizontal sync	OUT
30	VGA_VSYNC	VGA vertical sync	OUT
31	GND	Signal Ground	-
32	ONE_WIRE	One-Wire interface data/ power signal (open drain signal, Pullup 2k to VCC3V3)	IN/ OUT
33	SPI_CS0#	SPI chip select 0 (<i>low active</i>)	OUT
34	SPI_CS1#	SPI chip select 1 (<i>low active</i>)	OUT
35	SPI_SCK	SPI clock	OUT
36	SPI_MISO	SPI master in slave out	IN
37	SPI_MOSI	SPI master out slave in	OUT
38	GND	Signal Ground	-
39	VCC3V3	3,3V +/- 5% power supply, maximum current 300mA	-
40	VCC5V0	5V +/- 5% power supply, maximum current 300mA	-

8 Power Domains



The MSC Q7-TI8168 module uses different power domains which allows for efficient power management. Unused power rails can be switched off in order to reduce power consumption.

The diagram to the left shows all power domains (green). Affected functions are also shown (yellow), the specific signals can be found in section 2.7. The column named "Power Rail" reflects the power domains described in the diagram.